# X67BC81RT.L12

## 1 General information

The bus controller makes it possible to connect X2X Link I/O nodes to POWERLINK. It is also possible to operate the X2X Link cycle synchronously 1:1 or synchronous to POWERLINK using a prescaler.

Additional X2X Link I/O nodes (X67 modules or other modules based on X2X Link) can be connected using the integrated X2X Link connection. Mechanically, POWERLINK is connected via an IP67-rated standard D-coded M12 Ethernet connector.

POWERLINK is a standard protocol for Fast Ethernet with hard real-time characteristics. The POWERLINK Standardization Group (EPSG) ensures openness and continuous advancement. www.ethernet-powerlink.org

Ultrafast reACTION Technology makes it possible to control I/O channels with response times down to 1 µs. All of the commands that can be used for reACTION programs are provided as function blocks in special libraries (e.g. AsIORTI). Programming using the standard Function Block Diagram (FBD) editor in Automation Studio is compliant with IEC 61131-3.

- POWERLINK
- reACTION Technology module
- Integrated hub for efficient cabling
- 4 digital inputs
- 5 digital channels, configurable as inputs or outputs
- 2 analog inputs ±10 V
- 1 analog input ±10 V
- 1 ABR incremental encoder input 5 V
- 5 V and 24 V encoder power supply integrated in the encoder connector
- I/O configuration and firmware update via the fieldbus
- Integrated connection to local expansions via X2X Link for 250 additional modules
- Cycle time configurable starting at 200 µs for local expansions

## 2 Order data

| Order number | Short description | Figure |
|---|---|---|
| | **Bus controller modules** | |
| X67BC81RT.L12 | X67 bus controller, 2 POWERLINK interfaces, X2X Link power supply 15 W, reACTION Technology module, 2 digital inputs, 24 VDC, <1 µs, 3 digital channels, 5 VDC, <1 µs, configurable as inputs or outputs, 2 digital channels, 24 VDC, 0.4 A, <1 µs, configurable as inputs or outputs, 2 analog inputs ±10 V, 5 µs 200 kHz sampling frequency, 13-bit converter resolution including sign, configurable input filter, 1 analog output ±10 V, 2.5 µs, 13-bit converter resolution including sign, M12 connectors, high-density module |  |

Table 1: X67BC81RT.L12 - Order data

| Required accessories |
|---|
| See "Required cables and connectors" on page 9 and "Pinout" on page 12. |

# 3 Technical data

| Order number | X67BC81RT.L12 |
|---|---|
| **Short description** | |
| Bus controller | POWERLINK (V1/V2) controlled node |
| **General information** | |
| Inputs/Outputs | 4 digital inputs,<br>2 digital channels, configurable as inputs or outputs using software,<br>2 analog inputs,<br>1 analog output,<br>1 ABR input, also usable as 5 V differential inputs/outputs,<br>inputs with special function |
| Insulation voltage between channel and bus | 500 $V_{eff}$ |
| Nominal voltage | 24 VDC |
| B&R ID code | |
| Bus controller | 0xE2DC |
| Internal I/O module | 0xE2DF |
| Status indicators | I/O function per channel, supply voltage, bus function |
| Diagnostics | |
| Outputs | Yes, using LED status indicator and software |
| I/O power supply | Yes, using LED status indicator and software |
| Support | |
| reACTION-capable I/O channels | Yes |
| Connection type | |
| Fieldbus | M12, D-coded |
| X2X Link | M12, B-coded |
| Inputs/Outputs | M12, 5-pin, A-coded |
| Encoder | M12, 12-pin, A-coded |
| I/O power supply | M8, 4-pin |
| Power output | 15 W X2X Link power supply for I/O modules |
| Power consumption | |
| Fieldbus | 4.6 W |
| Internal I/O | 6 W |
| X2X Link power supply | 19.6 W at maximum power output for connected I/O modules |
| Application memory | |
| Type | 16 Mbit flash memory |
| Data retention | 20 years at 55°C |
| Guaranteed erase/write cycles | 100,000 |
| Certifications | |
| CE | Yes |
| ATEX | Zone 2, II 3G Ex nA IIA T5 Gc<br>IP67, Ta = 0 - Max. 60°C<br>TÜV 05 ATEX 7201X |
| UL | cULus E115267<br>Industrial control equipment |
| HazLoc | cCSAus 244665<br>Process control equipment<br>for hazardous locations<br>Class I, Division 2, Groups ABCD, T5 |
| EAC | Yes |
| **Interfaces** | |
| Fieldbus | POWERLINK (V1/V2) controlled node |
| Variant | 2x M12 circular connector (hub), 2x female connector on module |
| Line length | Max. 100 m between 2 stations (segment length) |
| Transfer rate | 100 Mbit/s |
| Transfer | |
| Physical layer | 100BASE-TX |
| Half-duplex | Yes |
| Full-duplex | No |
| Autonegotiation | Yes |
| Auto-MDI/MDIX | Yes |
| Hub propagation delay | 0.96 to 1 µs |
| Min. cycle time [1)] | |
| Fieldbus | 200 µs |
| X2X Link | 200 µs |
| Synchronization between bus systems possible | Yes |
| **Encoder power supply connector 8** | |
| 5 VDC | Module-internal, max. 0.3 A summation current |
| 24 VDC | Module-internal, max. 0.5 A summation current |
| **I/O power supply** | |
| Nominal voltage | 24 VDC |
| Voltage range | 18 to 30 VDC |
| Integrated protection | Reverse polarity protection |

Table 2: X67BC81RT.L12 - Technical data

| Order number | X67BC81RT.L12 |
|---|---|
| Power consumption | |
| Sensor/Actuator power supply | Max. 12 W [2] |
| **Sensor/Actuator power supply** | |
| Voltage | I/O power supply minus voltage drop for short-circuit protection |
| Voltage drop for short-circuit protection at 0.5 A | Max. 2 VDC |
| Summation current | Max. 0.5 A |
| Short-circuit proof | Yes |
| **ABR incremental encoder** | |
| Quantity | 1 |
| Encoder inputs | DI 5 to DI 7, 5 V, symmetrical<br>DI 1 to DI 4 and DI 8 to DI 9, 24 V, asymmetrical |
| Counter size | 32-bit |
| Input frequency | DI 1 to DI 7: 250 kHz<br>DI 8 and DI 9: 100 kHz |
| Evaluation | 4x |
| Encoder power supply | 5 V: Module-internal, max. 0.3 A<br>24 V: Module-internal, max. 0.5 A |
| Overload characteristics of encoder power supply | Short-circuit proof, overload-proof |
| **Digital inputs 5 VDC** | |
| Nominal voltage | 5 VDC |
| Input circuit | Differential |
| Insulation voltage between encoder and bus | 500 $V_{eff}$ |
| Input filter | |
| Hardware | No input filter |
| Software | Default 200 ns, configurable between 200 ns and 5 ms in 20 ns intervals |
| **Digital inputs 24 VDC** | |
| Nominal voltage | 24 VDC |
| Input characteristics per EN 61131-2 | Type 1 [3] |
| Input circuit | Sink |
| Input voltage | 24 VDC -15/+20% |
| Input filter | |
| Hardware | ≤50 ns |
| Software | Default 200 ns, configurable between 200 ns and 5 ms in 20 ns intervals |
| Input current at 24 VDC | |
| Channel 1 and 2 | Typ. 9 mA |
| Channel 3 and 4 | Typ. 3 mA |
| Channel 8 and 9 | Typ. 1 mA |
| Input resistance | |
| Channel 1 and 2 | Typ. 3 kΩ |
| Channel 3 and 4 | Typ. 8 kΩ |
| Channel 8 and 9 | Typ. 40 kΩ |
| Sensor power supply | 0.5 A summation current |
| Switching threshold | |
| Low | <5 VDC |
| High | <15 VDC |
| Insulation voltage between channel and bus | 500 $V_{eff}$ |
| **Analog inputs** | |
| Input | ±10 V |
| Input type | Single-ended |
| Digital converter resolution | 12-bit |
| Conversion time | 5 µs for both inputs |
| Output format | INT |
| Input protection | Protection against wiring with supply voltage |
| Open-circuit detection | Yes, using software |
| Reverse polarity protection | Yes |
| Permissible input signal | ±30 V |
| Output of digital value during overload | |
| Undershoot | 0x8001 |
| Overshoot | 0x7FFF |
| Conversion procedure | Successive approximation |
| Max. error | |
| Gain | 0.1% [4] |
| Offset | 0.05% [5] |
| Max. drift at 25°C | |
| Gain | 0.01%/°C [4] |
| Offset | 0.0075% / °C [5] |
| Crosstalk between channels | -70 dB |
| Nonlinearity | <0.0062% [5] |
| Insulation voltage between channel and bus | 500 $V_{eff}$, 1 min |
| **Digital outputs 5 VDC** | |
| Output protection | Short-circuit protection |
| Variant | Differential |
| Nominal voltage | 5 VDC |

Table 2: X67BC81RT.L12 - Technical data

| Order number | X67BC81RT.L12 |
|---|---|
| Output current | Max. 65 mA [6] |
| Diagnostic status | Output monitoring |
| Switching frequency | Max. 500 kHz |
| **Digital outputs 24 VDC** | |
| Nominal voltage | 24 VDC |
| Nominal output current | 0.4 A |
| Variant | Push/Pull |
| Output protection | Thermal shutdown in the event of overcurrent or short circuit |
| Braking voltage when switching off inductive loads | 50 VDC |
| Diagnostic status | Overload monitoring |
| Switch-on in the event of overload shutdown or short-circuit shutdown | Approx. 25 ms |
| Peak short-circuit current | <1 A |
| Switching voltage | 24 VDC (-15/+20%) |
| Switching frequency | |
| Resistive load | Max. 100 kHz |
| Inductive load | Max. 100 kHz |
| Switching delay | |
| 0 → 1 | <1 µs |
| 1 → 0 | <1 µs |
| Insulation voltage between channel and bus | 500 $V_{eff}$ |
| **Analog outputs** | |
| Output | ±10 V |
| Digital converter resolution | 12-bit |
| Conversion time | 2 µs |
| Settling time on output change over entire range | 2.5 µs |
| Switch on/off behavior | Internal enable relay for startup |
| Max. error | |
| Gain | 0.15% [4] |
| Offset | 0.05% [5] |
| Output protection | Short-circuit proof |
| Output format | Example: INT 0x8001 - 0x7FFF / 1 LSB = 0x0010 = 4.882 mV |
| Load per channel | Max. ±10 mA, load ≥1 kΩ |
| Output filter | First-order low-pass filter / cutoff frequency 2.5 kHz |
| Max. gain drift | 0.012%/°C [4] |
| Max. offset drift | 0.001%/°C [5] |
| Error caused by load change | Max. 0.01%, from 10 MΩ → 1 kΩ, resistive |
| Nonlinearity | <0.15% [5] |
| Insulation voltage between channel and bus | 500 $V_{eff}$, 1 min |
| Output response when the power supply is switched on/off | An enable relay is switched on at a defined value ≠ 0, default setting = 10 kΩ to GND |
| Short-circuit proof | |
| Current limiting | ±40 mA |
| To actuator or I/O power supply | Yes |
| To GND | Yes |
| Max. error at 25°C and 10 kΩ load | |
| Gain | 0.15% |
| Offset | 0.05% |
| **Electrical properties** | |
| Electrical isolation | Bus isolated from POWERLINK and channel<br>Channel not isolated from channel |
| **Operating conditions** | |
| Mounting orientation | |
| Any | Yes |
| Installation elevation above sea level | |
| 0 to 2000 m | No limitation |
| >2000 m | Reduction of ambient temperature by 0.5°C per 100 m |
| Degree of protection per EN 60529 | IP67 |
| **Ambient conditions** | |
| Temperature | |
| Operation | -25 to 60°C |
| Derating | - |
| Storage | -40 to 85°C |
| Transport | -40 to 85°C |
| **Mechanical properties** | |
| Dimensions | |
| Width | 53 mm |
| Height | 155 mm |
| Depth | 42 mm |

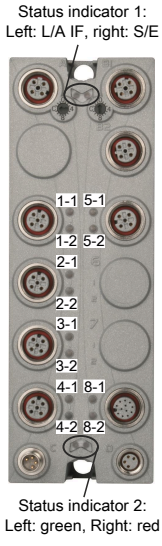
Table 2: X67BC81RT.L12 - Technical data

| Order number | X67BC81RT.L12 |
|---|---|
| Weight | 320 g |
| Torque for connections | |
| M8 | Max. 0.4 Nm |
| M12 | Max. 0.6 Nm |

Table 2: X67BC81RT.L12 - Technical data

1) The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring.
2) The power consumption of the sensors and actuators connected to the module is not permitted to exceed 12 W.
3) Only channels 1 to 4
4) Based on the current output value.
5) Based on the total output value.
6) For differential output voltage depending on the output current, see section "Differential output"

# 4 LED status indicators

| Figure | LED | Color | Status | Description |
|---|---|---|---|---|
|  | **Status indicator 1**: Status indicator for POWERLINK bus controller | | | |
| | L/A IF | Green | On | A link to the peer station has been established. |
| | | | Blinking | A link to the peer station has been established. Indicates Ethernet activity is taking place on the bus. |
| | S/E | Green/Red | - | Status/Error LED:<br>The statuses of this LED are described in section "Status/Error LED "S/E"" on page 5. |
| | **I/O LEDs** | | | |
| | 1-1/2 | Green | - | Input status of the corresponding channel |
| | 2-1/2 and 3-1/2 | Status indicator for the corresponding analog output | | |
| | | Green | On | Analog-to-digital converter running |
| | | | Blinking | Input signal overflow or underflow |
| | | | Off | Open circuit or sensor is disconnected. |
| | 5-1/2 and 8-1/2 | Status indicator for input/output | | |
| | | Orange | On | Output status of channel x |
| | | Green | On | Input status of channel x |
| | | Orange/Green | - | One I/O channel is configured as an input and one as an output. Both channels are active. |
| | 4-1 | Status indicator for the corresponding analog output | | |
| | | Orange | On | Lit as soon as the enable relay is activated (i.e. a value ≠ 0 is output) |
| | | | Off | The enable relay has not yet been activated (no value ≠ 0 has been output yet). |
| | **Status indicator 2**: Status indicator for module function | | | |
| | Left | Green | Off | No power to module |
| | | | Single flash | RESET mode |
| | | | Blinking | PREOPERATIONAL mode |
| | | | On | RUN mode |
| | Right | Red | Off | No power to the module or everything is OK. |
| | | | On | Error or reset state (reACTION program using functions or channels that are not permitted on this hardware) |
| | | | Single flash | Level monitoring of digital outputs activated or cycle time violation (reACTION program cannot be executed within the configured cycle time) |
| | | | Double flash | Supply voltage not in valid range or no reACTION program loaded |

### Status/Error LED "S/E"

The Status/Error LED is a green/red dual LED. The color green (status) is superimposed on the color red (error).

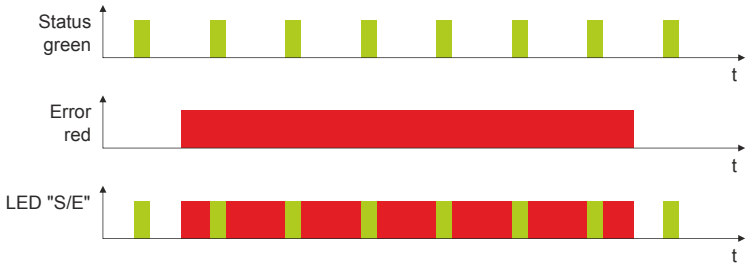
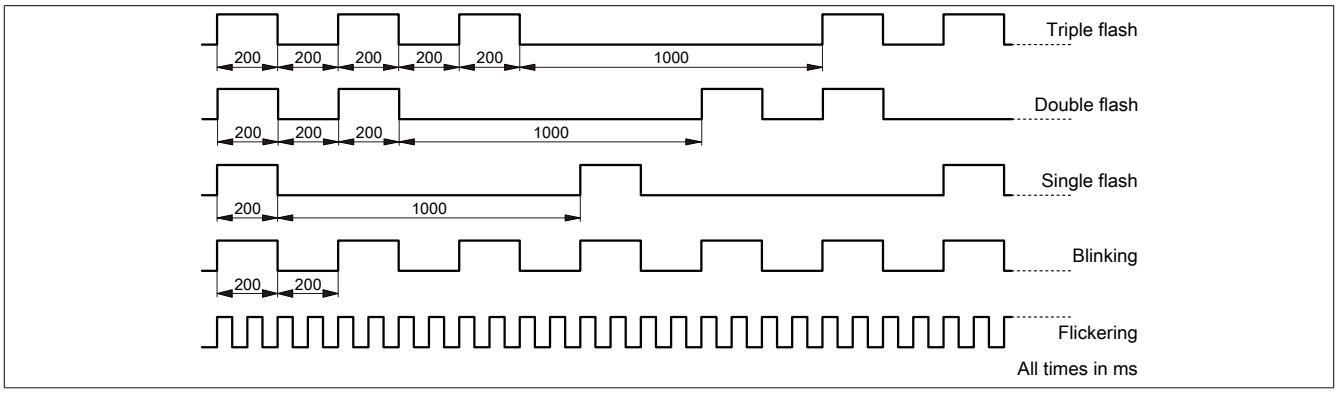
| Red - Error | Description |
|---|---|
| On | The controlled node (CN) is in an error state (failed Ethernet frames, increased number of collisions on the network, etc.).<br>If an error occurs in the following states, then the green LED blinks over the red LED:<br>• PRE_OPERATIONAL_1<br>• PRE_OPERATIONAL_2<br>• READY_TO_OPERATE<br>  <br><br>Note:<br>• Several red blinking signals are displayed immediately after the device is switched on. This is not an error, however.<br>• The LED is lit red for CNs with configured physical node number 0 but that have not yet been assigned a node number via dynamic node allocation (DNA). |

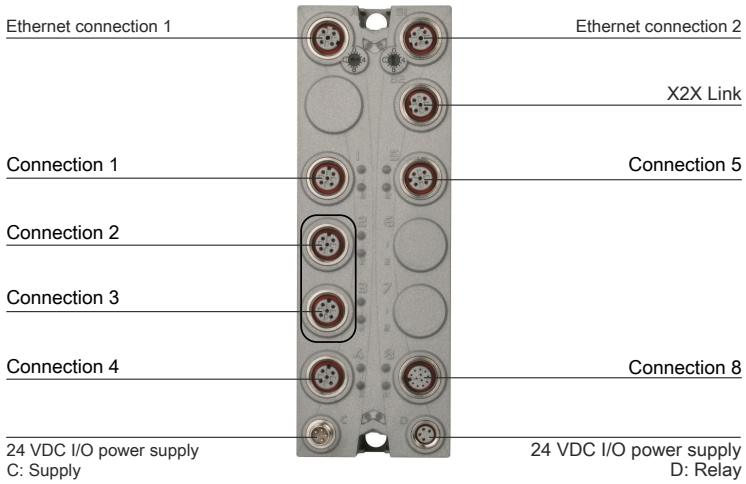
Table 3: Red Status/Error LED: LED indicates an error

| Color green - Status | Description |
|---|---|
| Off | No power supply or mode NOT_ACTIVE.<br>The controlled node (CN) is either not supplied with power, or it is in state NOT_ACTIVE. The CN waits in this state for about 5 seconds after a restart. Communication is not possible with the CN. If no POWERLINK communication is detected during these 5 seconds, the CN enters state BASIC_ETHERNET (flickering).<br>If POWERLINK communication is detected before this time expires, however, the CN immediately enters state PRE_OPERATIONAL_1. |
| Green flickering (approx. 10 Hz) | Mode BASIC_ETHERNET.<br>The CN has not detected any POWERLINK communication. In this state, it is possible to communicate directly with the CN (e.g. with UDP, IP, etc.)<br>If communication POWERLINK is detected in this state, the CN switches to PRE_OPERATIONAL_1. |
| Single flash (approx. 1 Hz) | Mode PRE_OPERATIONAL_1.<br>When operating on a POWERLINK V1 manager, the CN switches directly to PRE_OPERATIONAL_2.<br>When operated on a POWERLINK V2 manager, the CN waits until an SoC frame is received and then switches to the PRE_OPERATIONAL_2 state. |
| Double flash (approx. 1 Hz) | Mode PRE_OPERATIONAL_2.<br>The CN is normally configured by the manager in this state. It is then switched to state READY_TO_OPERATE by command (POWERLINK V2) or by setting the "data valid" flag in the output data (POWERLINK V1). |
| Triple flash (approx. 1 Hz) | Mode READY_TO_OPERATE.<br>In network POWERLINK V1, the CN switches automatically to OPERATIONAL as soon as input data is present.<br>In a POWERLINK V2 network, the manager switches to the OPERATIONAL state by issuing a command. |
| On | Mode OPERATIONAL.<br>The PDO mapping is active and cyclic data is evaluated. |
| Blinking (approx. 2.5 Hz) | Mode STOPPED.<br>Output data is not being output, and no input data is being provided. It is only possible to switch to or leave this state after the manager has given the appropriate command. |

Table 4: Status/Error LED lit green: LED indicating operating state



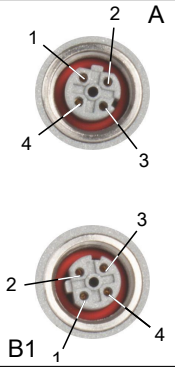
# 5 Operating and connection elements




| | |
|---|---|
| Connection 1: | 2x digital inputs |
| Connections 2 + 3: | 2x analog inputs (or 2x 1 analog input) |
| Connection 4: | 1x analog output |
| Connection 5: | 2x digital inputs/outputs |
| Connection 8: | 2x digital inputs (24 VDC) and 3x digital inputs/outputs (5 VDC) |

# 6 POWERLINK interface

The module is connected to the network using pre-assembled cables. The connection is made using M12 circular connectors.

| Connection | Pinout | | |
|---|---|---|---|
|  | Pin | Name | |
| | 1 | TXD | Transmit data |
| | 2 | RXD | Receive data |
| | 3 | TXD\ | Transmit data\ |
| | 4 | RXD\ | Receive data\ |
|  | Shield connection made via threaded insert in the module<br><br>A → D-keyed (female), input<br>B1 → D-keyed (female), output | | |

## Information:

**The color of the wires used in field-assembled cables for connecting to the fieldbus interface may deviate from the standard.**

**It is extremely important to make sure that the pinout is correct (see X67 section "Accessories - POWERLINK cables" in the X67 user's manual).**

## 6.1 Cabling guidelines for bus controllers with Ethernet cables

Some X67 system bus controllers are based on Ethernet technology. POWERLINK cables supplied by B&R can be used for wiring.

| Model number | Connection type |
|---|---|
| X67CA0E41.xxxx | Attachment cables - RJ45 to M12 |
| X67CA0E61.xxxx | Connection cables - M12 to M12 |

The following cabling guidelines must be observed:

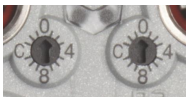
- Use Cat 5 SFTP cables.
- Observe the minimum cable bend radius (see data sheet for the cable).

## Information:

**Using POWERLINK cables supplied by B&R (X67CA0E61.xxxx and X67CA0E41.xxxx) satisfies product standard EN 61131-2.**

**The customer must implement additional measures in the event of further requirements.**

## 6.2 POWERLINK node number

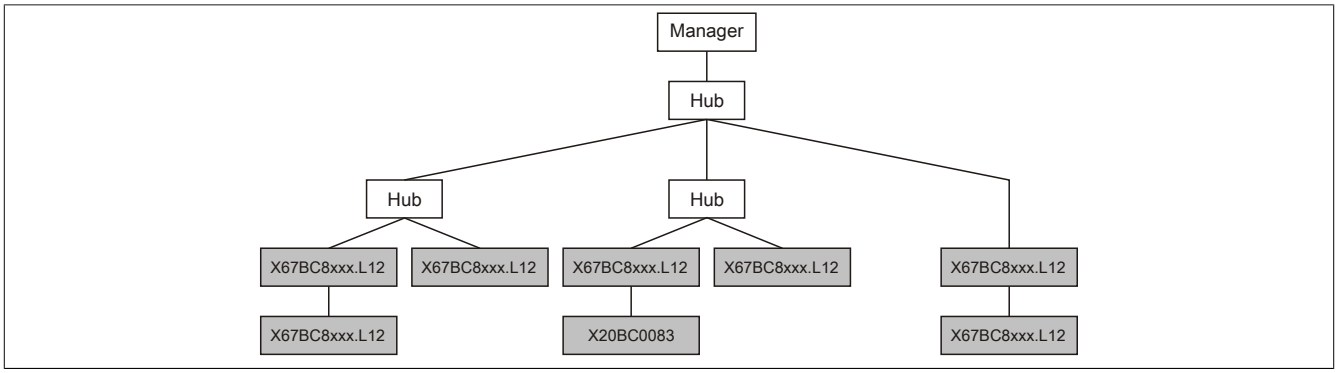



The node number for the POWERLINK node is set using the two number switches.

| Switch position | Description |
|---|---|
| 0x00 | Only permitted when operating the POWERLINK node in DNA mode. |
| 0x01 - 0xEF | Node number of the POWERLINK node. Operation as a controlled node. |
| 0xF0 - 0xFF | Reserved, switch position not permitted. |

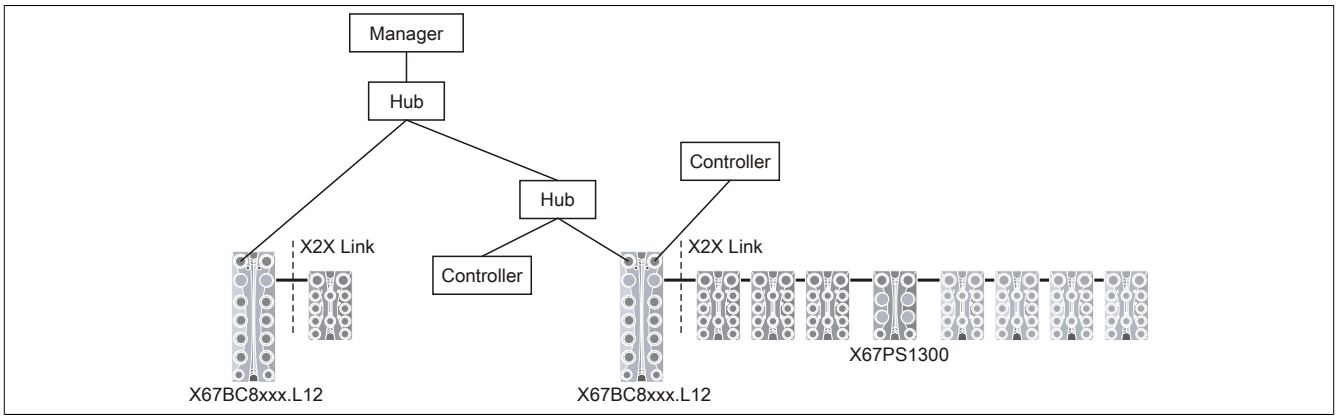
## 6.3 Integration in a POWERLINK network

This bus controller can be used in a tree or line topology as follows:




## 6.4 System configuration

A digital mixed module is already integrated in the bus controller. Up to 250 I/O modules can be connected to the bus controller.

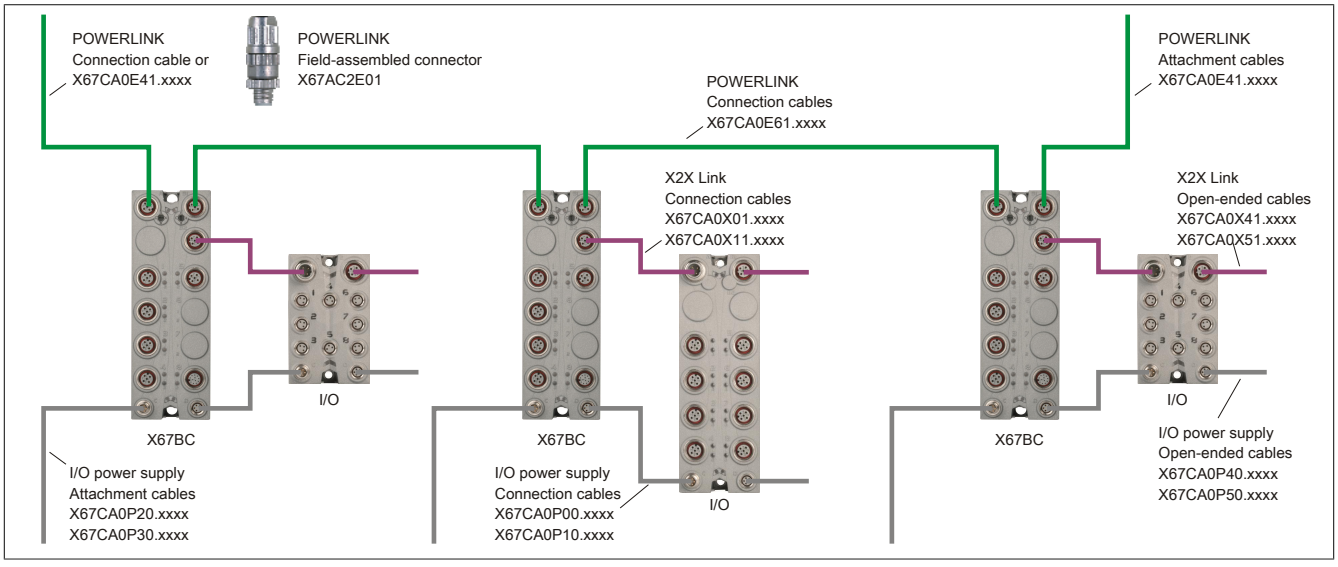



## Information:

**15 W are provided by the bus controller for additional X67 modules or other X2X Link-based modules.**

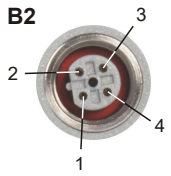
**System supply module X67PS1300 is needed for additional power. This system supply module provides 15 W for additional modules. Each one should be mounted in the middle of the modules that are to be supplied with power.**

## 6.5 Required cables and connectors



# 7 X2X Link

Additional modules can be connected to the bus controller via X2X Link using pre-assembled cables. The connection is made using an M12 circular connector.

| Connection | Pinout | |
|---|---|---|
|  | **Pin** | **Name** |
| | 1 | X2X+ |
| | 2 | X2X |
| | 3 | X2X⊥ |
| | 4 | X2X\ |
| | Shield connection made via threaded insert in the module<br><br>B2 → B-keyed (female), output | |

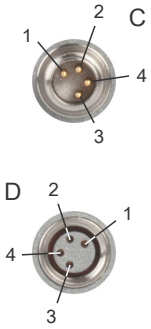
# 8 24 VDC I/O power supply

The I/O power supply is connected via M8 connectors C and D. The power supply is connected via connection C (male). Connector D (female) is used to route the power supply to other modules.

The fieldbus / X2X Link power supply and I/O power supply are supplied separately via pins 1 and 2.

## Information:

**The maximum permissible current for the I/O power supply is 8 A (4 A per pin).**

| Connection | Pinout | | |
|---|---|---|---|
|  | **Pin** | **Connector C (male)** | **Connector D (female)** |
| | 1 | 24 VDC fieldbus / X2X Link | 24 VDC I/O |
| | 2 | 24 VDC I/O | 24 VDC I/O |
| | 3 | GND | GND |
| | 4 | GND | GND |
| | C → Connector (male) in module, feed for I/O power supply<br>D → Connector (female) in module, routing of I/O power supply | | |

## Information:

**If the summation current of the outputs is >4 A, current must also be supplied via connector D, pin 2.**

# 9 Local I/O channels

The following table provides an overview of the connections to the I/O channels and their properties.

### Digital inputs/outputs

| Connection | Pin | Channel | Description |
|---|---|---|---|
| X1 | 2 | DI 1 | 24 VDC, sink, ≤50 ns, configurable software filter |
| | 4 | DI 2 | 24 VDC, sink, ≤50 ns, configurable software filter |
| X5 | 2 | DI 3 / DO 3 | DI: 24 VDC, sink, ≤50 ns, configurable software filter<br>DO: 24 VDC, 0.4 A, push-pull, <1 µs |
| | 4 | DI 4 / DO 4 | DI: 24 VDC, sink, ≤50 ns, configurable software filter<br>DO: 24 VDC, 0.4 A, push-pull, <1 µs |
| X8 | 5, 6 | DI 5 / DO 5 | DI: 5 VDC module, differential: Type RS485<br>DO: 5 VDC, 100 mA, differential: Type RS485 (tri-state, if inactive) |
| | 8, 1 | DI 6 / DO 6 | DI: 5 VDC module, differential: Type RS485<br>DO: 5 VDC, 100 mA, differential: Type RS485 (tri-state, if inactive) |
| | 3, 4 | DI 7 / DO 7 | DI: 5 VDC module, differential: Type RS485<br>DO: 5 VDC, 100 mA, differential: Type RS485 (tri-state, if inactive) |
| | 2 | DI 8 | 24 VDC, sink, ≤50 ns, configurable software filter |
| | 7 | DI 9 | 24 VDC, sink, ≤50 ns, configurable software filter |

### Analog inputs

| Connection | Pin | Channel | Description |
|---|---|---|---|
| X2[1)] | 2 | AI 1 | ±10 V, 12-bit, 5 µs |
| | 4 | AI 2 | ±10 V, 12-bit, 5 µs |
| X3[1)] | 2 | AI 2 | ±10 V, 12-bit, 5 µs |
| | 4 | AI 1 | ±10 V, 12-bit, 5 µs |

1) The connections 2 and 3 are cross-connected with each other (see "Analog inputs - Connection examples" on page 14).

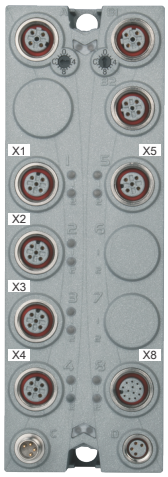
### Analog output

| Connection | Pin | Channel | Description |
|---|---|---|---|
| X4 | 1, 3 | AO 1 | ±10 V, 12-bit, 2 µs |

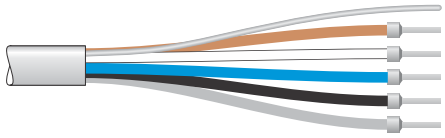
The following sections describe assigning I/O channels in a reACTION program:

| I/O channels | Assignment |
|---|---|
| Digital I/O channels | Assignment of digital inputs/outputs |
| Analog input channels | Assignment of analog inputs |
| Analog output channel | Assignment of analog output |

# 10 Pinout




X1
M12 ①

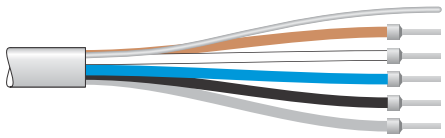


| Shield | |
|---|---|
| 1 | +24 VDC |
| 2 | DI 1 |
| 3 | GND |
| 4 | DI 2 |
| 5 | NC |

X2
M12 ①

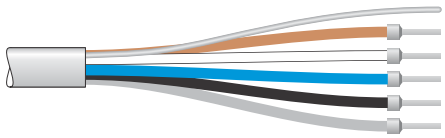
| Shield | |
|---|---|
| 1 | +24 VDC |
| 2 | AI 1 |
| 3 | GND |
| 4 | AI 2 |
| 5 | Shield |

X3
M12 ①



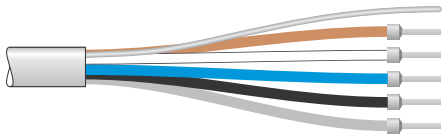
| Shield | |
|---|---|
| 1 | +24 VDC |
| 2 | AI 2 |
| 3 | GND |
| 4 | AI 1 |
| 5 | Shield |

X4
M12 ①



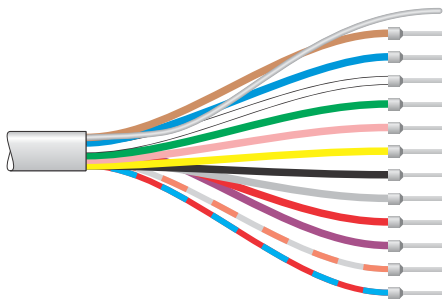
| Shield | |
|---|---|
| 1 | AO + 1 |
| 2 | +24 VDC |
| 3 | AO - 1 (GND) |
| 4 | GND |
| 5 | Shield |

X5
M12 ①



| Shield | |
|---|---|
| 1 | +24 VDC |
| 2 | DI 3 / DO 3 |
| 3 | GND |
| 4 | DI 4 / DO 4 |
| 5 | NC |

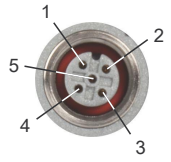
X8
M12 ②



| Shield | |
|---|---|
| 1 | DI 6\ / DO 6\ |
| 2 | DI 8 |
| 3 | DI 7 / DO 7 |
| 4 | DI 7\ / DO 7\ |
| 5 | DI 5 / DO 5 |
| 6 | DI 5\ / DO 5\ |
| 7 | DI 9 |
| 8 | DI 6 / DO 6 |
| 9 | NC |
| 10 | +5 VDC |
| 11 | +24 VDC |
| 12 | GND |

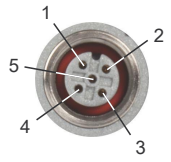
① X67CA0A41.xxxx: M12 straight sensor cable
X67CA0A51.xxxx: M12 angled sensor cable
② X67CA0I41.xxxx: Straight multi-function cable
X67CA0I51.xxxx: Angled multi-function cable

## 10.1 Connection X1

| M12, 5-pin | Pinout | |
|---|---|---|
| Connection 1 | **Pin** | **Name** |
|  | 1 | 24 VDC sensor supply[1)] |
| | 2 | DI 1 |
| | 3 | GND |
| | 4 | DI 2 |
| | 5 | NC |
| | 1) Sensors are not permitted to be supplied externally.<br>Shield connection made via threaded insert in the module | |

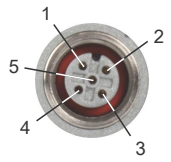


## 10.2 Connection X2/X3

| M12, 5-pin | Pinout | | |
|---|---|---|---|
| Connection 2/3 | **Pin (X2)** | **Pin (X3)** | **Name** |
|  | 1 | 1 | 24 VDC sensor supply[1)] |
| | 2 | 4 | AI 1 |
| | 3 | 3 | GND |
| | 4 | 2 | AI 2 |
| | 5 | 5 | Shield[2)] |
| | 1) Sensors are not permitted to be supplied externally.<br>2) Shielding also provided by threaded insert in the module. | | |

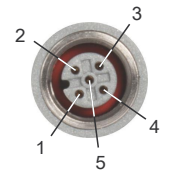


## 10.3 Connection X4

| M12, 5-pin | Pinout | |
|---|---|---|
| Connection 4 | **Pin** | **Name** |
|  | 1 | AO + 1 |
| | 2 | 24 VDC actuator power supply[1)] |
| | 3 | AO - 1 (GND) |
| | 4 | GND |
| | 5 | Shield[2)] |
| | 1) Actuators are not permitted to be supplied externally.<br>2) Shielding also provided by threaded insert in the module. | |

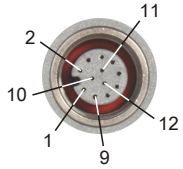


## 10.4 Connection X5

| M12, 5-pin | Pinout | |
|---|---|---|
| Connection 5 | **Pin** | **Name** |
|  | 1 | 24 VDC sensor/actuator power supply[1)] |
| | 2 | DI 3 / DO 3 |
| | 3 | GND |
| | 4 | DI 4 / DO 4 |
| | 5 | NC |
| | 1) Sensors/Actuators are not permitted to be supplied externally.<br>Shield connection made via threaded insert in the module | |



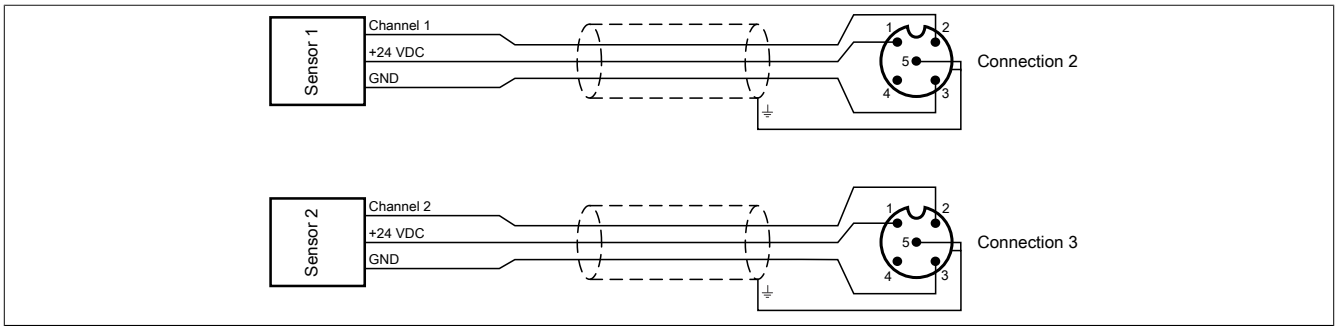
## 10.5 Connection X8

| M12, 12-pin | Pinout | |
|---|---|---|
| | **Pin** | **Name** |
| Connection 8 | 1 | DI 6\ / DO 6\ |
|  | 2 | DI 8 |
| | 3 | DI 7 / DO 7 |
| | 4 | DI 7\ / DO 7\ |
| | 5 | DI 5 / DO 5 |
| | 6 | DI 5\ / DO 5\ |
| | 7 | DI 9 |
| | 8 | DI 6 / DO 6 |
| | 9 | NC |
| | 10 | 5 VDC encoder power supply[1)] |
| | 11 | 24 VDC encoder power supply[1)] |
| | 12 | GND |
| | 1) Encoder power supply is not permitted to be supplied externally.<br>Shield connection made via threaded insert in the module | |

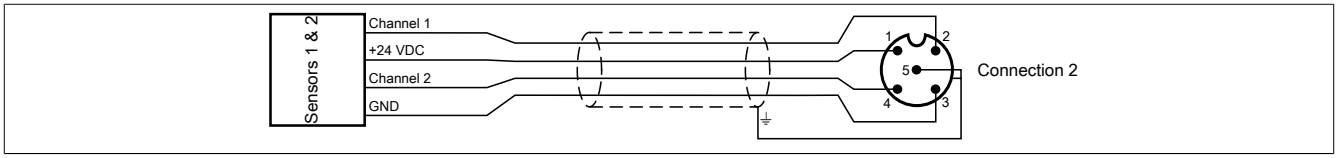
# 11 Analog inputs - Connection examples

Connections X2 and X3 make 2 analog inputs available. The connections are directly connected with each other (see input circuit diagram "Analog inputs (X2/X3)" on page 16) with the result that they have to be considered together. Depending on the pinout of the sensors, either the two signals can be processed by the module on the same connection or one signal per connection.

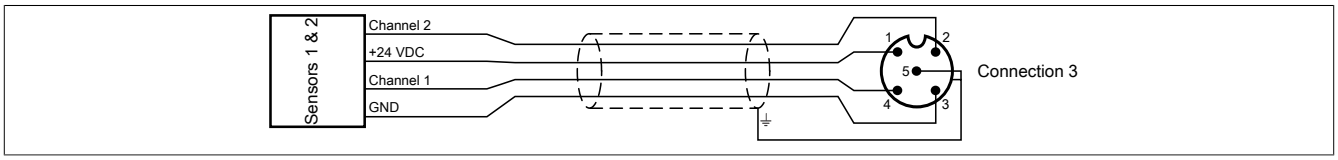
### Connection example 1




### Connection example 2

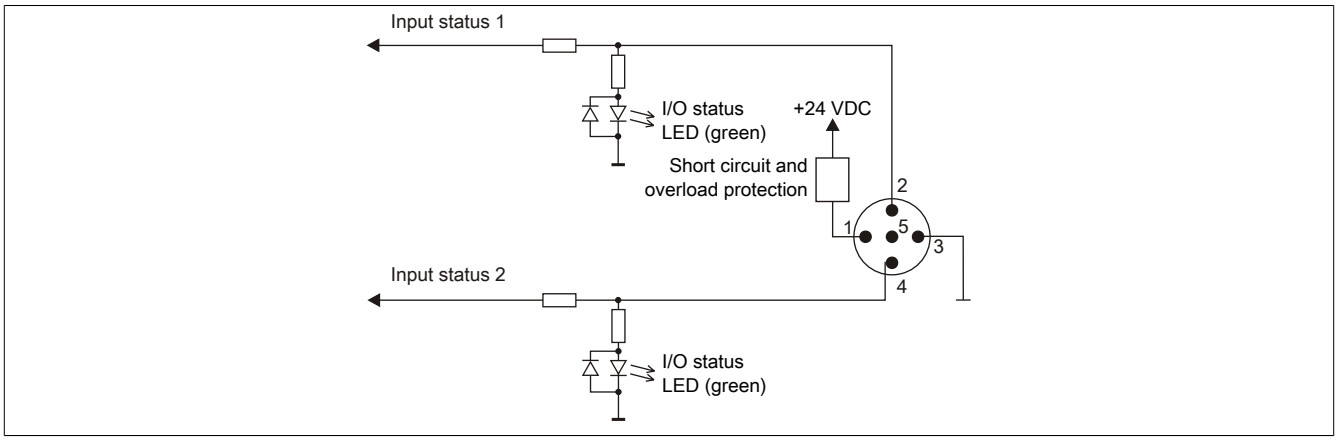



### Connection example 3

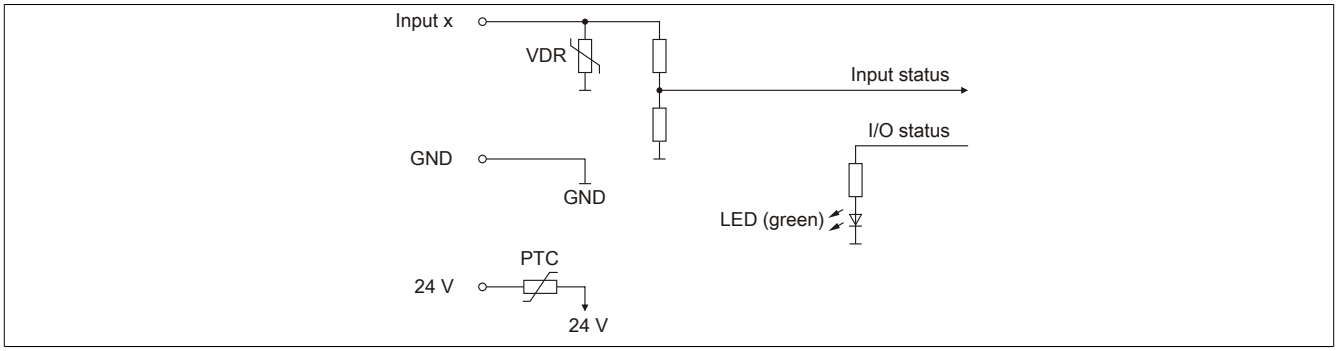


# 12 Input/Output circuit diagram

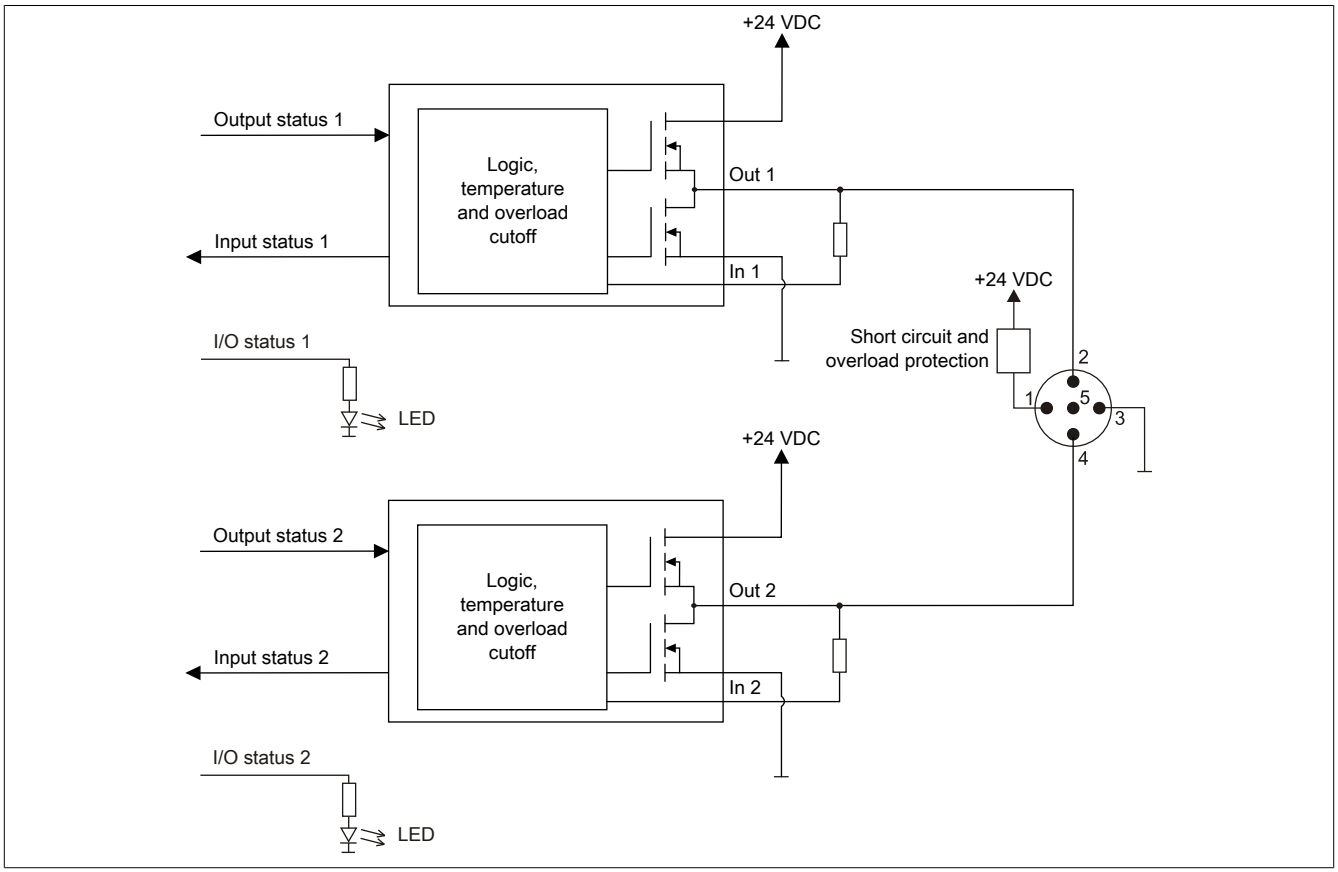
## 12.1 Digital inputs (X1)



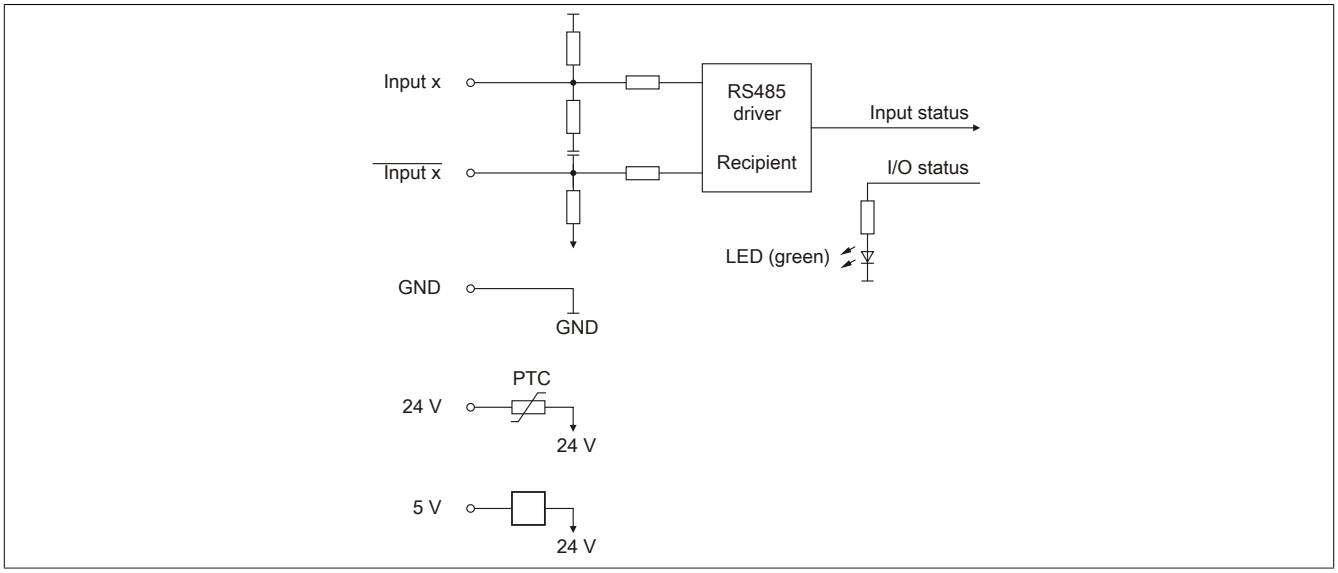

## 12.2 Digital inputs (X8)

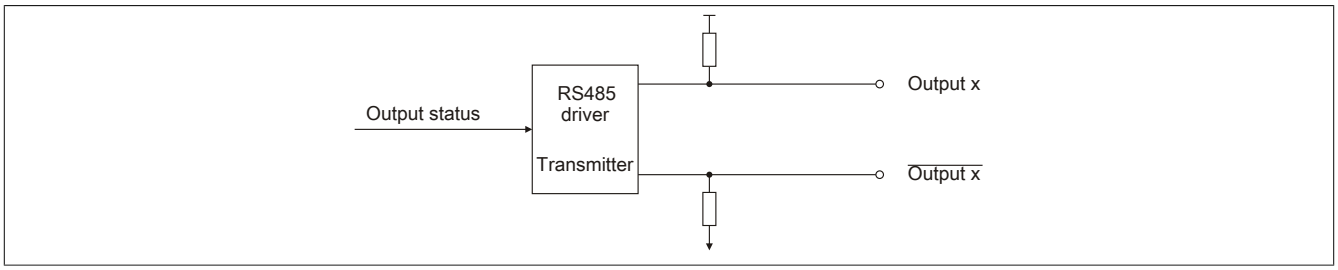



## 12.3 Digital inputs/outputs (X5)



## 12.4 Digital inputs/outputs (X8)

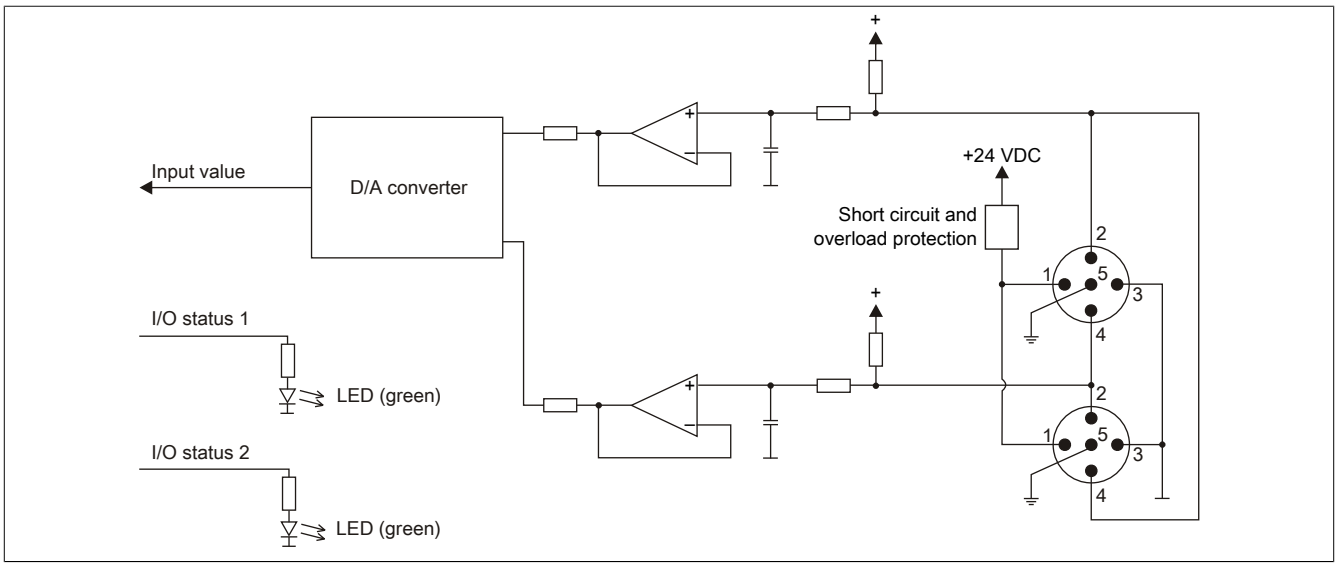


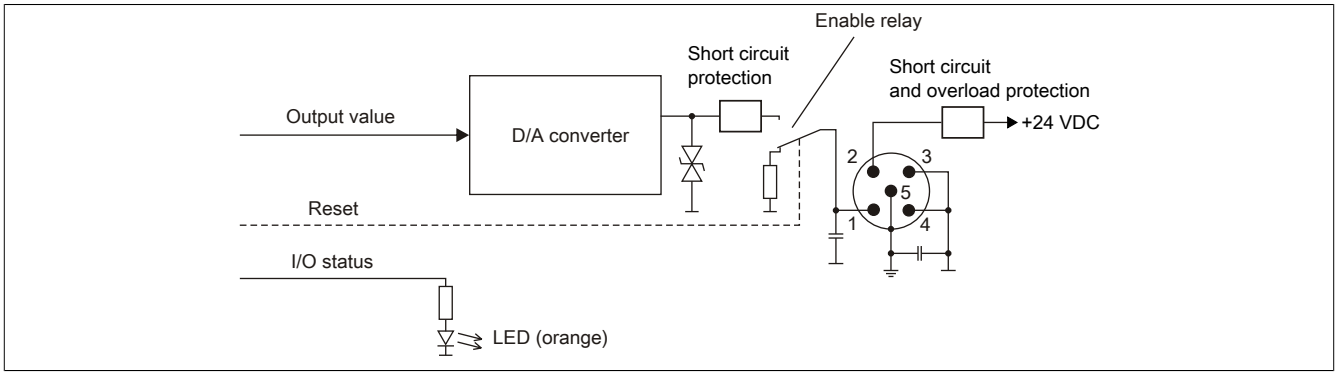

# Information:

**The digital inputs and outputs of the X8 connection were designed for signal levels of 5 VDC.**

## 12.5 Analog inputs (X2/X3)

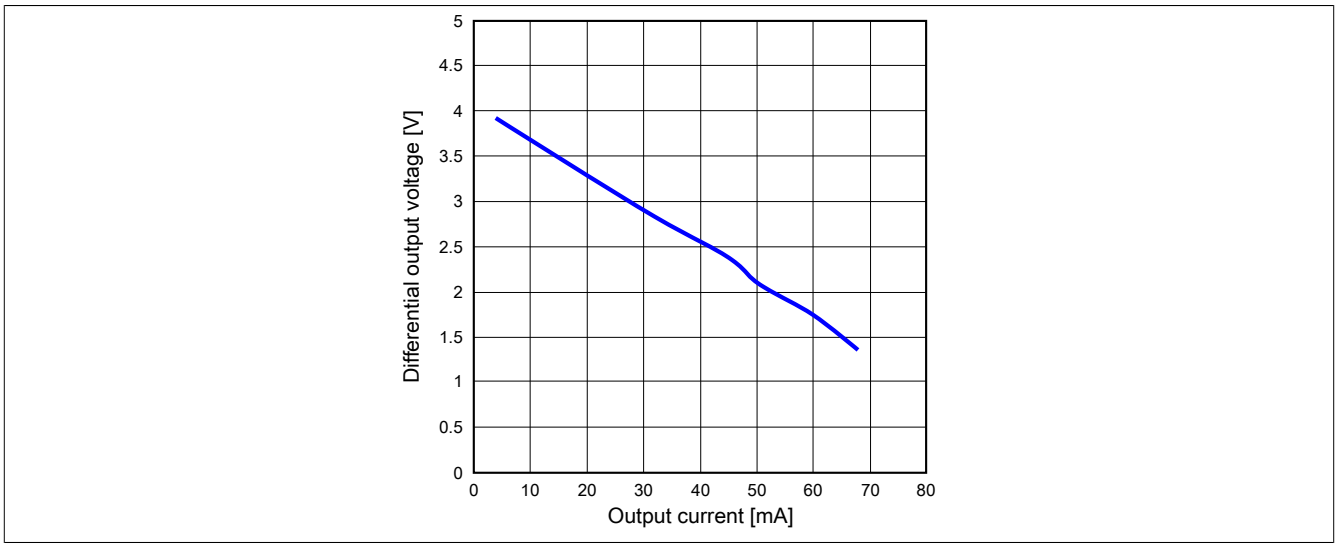


### 12.6 Analog output (X4)




## 13 Differential output

The following diagram shows that the differential output voltage sinks when the output current rises.



# 14 Register description

## 14.1 Function model 0 - "reACTION"

When using the "reACTION" function model, an individual reACTION program must be created for the module. This program will be executed by the reACTION module later on, not by the CPU. This allows individual machine tasks to be managed decentrally and with a very short response time.

The inputs and outputs of a reACTION module can only be operated by an enabled reACTION program. Interaction registers allow information to be exchanged between the CPU and the reACTION program in the module.

In addition to communication with the CPU, the cyclic interaction registers can also be used for "cross-mapping". In this way, inputs/outputs can also be read/controlled by external modules across the entire X2X Link or POWERLINK network.

| Register | Name | Data type | Read | | Write | |
|---|---|---|---|---|---|---|
| | | | Cyclic | Acyclic | Cyclic | Acyclic |
| **Module - Configuration** | | | | | | |
| 131 | CfO_LedEnable_AI | USINT | | | | • |
| **Module communication** | | | | | | |
| 158 | ModuleStatus | UINT | | • | | |
| 162 | DigitalStatus | UINT | | • | | |
| **reACTION - Configuration** | | | | | | |
| 772 | ReActionCycleTimeValue | UDINT | | | | • |
| 780 | ReActionCycleTimeMultiplier | UDINT | | | | • |
| Index*8 + 508 | CfO_PARType01<br>CfO_PARType[02…04] | UDINT | | | | • |
| **reACTION - Communication** | | | | | | |
| 129 | reACTION - Control byte | USINT | | | • | |
| | RTEnable | Bit 0 | | | | |
| | RTHardwareWarningQuit | Bit 2 | | | | |
| 145 | reACTION - Status byte | USINT | • | | | |
| | RTEngineRun | Bit 0 | | | | |
| | RTCycleTimeOverrun | Bit 1 | | | | |
| | RTHardwareWarning | Bit 2 | | | | |
| | RTFileInvalid | Bit 4 | | | | |
| | RTFunctionInvalid | Bit 5 | | | | |
| | RTInstanceInvalid | Bit 6 | | | | |
| | RTFileNotLoaded | Bit 7 | | | | |
| 154 | RTCycleCounter | UINT | • | | | |
| 150 | RTCycleTime | UINT | • | | | |
| **reACTION - Interaction** | | | | | | |
| Index*8 + 4095 | PAR01<br>PAR[02...32] | (U)SINT | | | • | |
| | PAR01_Bit1<br>PAR[02...32]_Bit1 | Bit 0 | | | | |
| | PAR01_Bit2<br>PAR[02...32]_Bit2 | Bit 1 | | | | |
| | PAR01_Bit3<br>PAR[02...32]_Bit3 | Bit 2 | | | | |
| | PAR01_Bit4<br>PAR[02...32]_Bit4 | Bit 3 | | | | |
| | PAR01_Bit5<br>PAR[02...32]_Bit5 | Bit 4 | | | | |
| | PAR01_Bit6<br>PAR[02...32]_Bit6 | Bit 5 | | | | |
| | PAR01_Bit7<br>PAR[02...32]_Bit7 | Bit 6 | | | | |
| | PAR01_Bit8<br>PAR[02...32]_Bit8 | Bit 7 | | | | |
| Index*8 + 4094 | PAR01<br>PAR[02...32] | (U)INT | | | • | |
| Index*8 + 4092 | PAR01<br>PAR[02...32] | (U)DINT | | | • | |

| Register | Name | Data type | Read | | Write | |
|---|---|---|---|---|---|---|
| | | | Cyclic | Acyclic | Cyclic | Acyclic |
| Index*8<br>+ 5119 | RES01<br>RES[02…32] | (U)SINT | • | | | |
| | RES01_Bit1<br>RES[02…32]_Bit1 | Bit 0 | | | | |
| | RES01_Bit2<br>RES[02…32]_Bit2 | Bit 1 | | | | |
| | RES01_Bit3<br>RES[02…32]_Bit3 | Bit 2 | | | | |
| | RES01_Bit4<br>RES[02…32]_Bit4 | Bit 3 | | | | |
| | RES01_Bit5<br>RES[02…32]_Bit5 | Bit 4 | | | | |
| | RES01_Bit6<br>RES[02…32]_Bit6 | Bit 5 | | | | |
| | RES01_Bit7<br>RES[02…32]_Bit7 | Bit 6 | | | | |
| | RES01_Bit8<br>RES[02…32]_Bit8 | Bit 7 | | | | |
| Index*8<br>+ 5118 | RES01<br>RES[02…32] | (U)INT | • | | | |
| Index*8<br>+ 5116 | RES01<br>RES[02…32] | (U)DINT | • | | | |
| Index*8<br>+ 6140 | PVAR1<br>PVAR[2...256] | DINT | | | | • |
| Index*8<br>+ 6140 | RVAR1<br>RVAR[2...256] | DINT | | • | | |
| **reACTION - Function block configuration** | | | | | | |
| 1028 | CfO_Config_ABR1 | UDINT | | | | • |
| 1036 | CfO_ScalingIncrements_ABR1 | UDINT | | | | • |
| 1044 | CfO_ScalingUnits_ABR1 | UDINT | | | | • |
| 1052 | CfO_ChannelMapping1_ABR1 | UDINT | | | | • |
| 1060 | CfO_ChannelMapping2_ABR1 | UDINT | | | | • |

## 14.2 Function model 254 - "Direct I/O"

In the "Direct I/O" function model, a special reACTION program is executed in the module in order to manage the I/O. In addition, cyclic registers are used to exchange information with the CPU. This reproduces the behavior of a standard module.

| Register | Name | Data type | Read | | Write | |
|---|---|---|---|---|---|---|
| | | | Cyclic | Acyclic | Cyclic | Acyclic |
| **Module - Configuration** | | | | | | |
| 131 | CfO_LedEnable_AI | USINT | | | | • |
| **Module communication** | | | | | | |
| 129 | Status acknowledgment | USINT | | | • | |
| | RTHardwareWarningQuit | Bit 2 | | | | |
| 145 | Status - Composite message | USINT | • | | | |
| | RTHardwareWarning | Bit 2 | | | | |
| 158 | ModuleStatus | UINT | • | | | |
| | SensorSupplyX5Ok | Bit 2 | | | | |
| | SensorSupplyX1Ok | Bit 3 | | | | |
| | SensorSupplyX23Ok | Bit 4 | | | | |
| | SensorSupplyX48Ok | Bit 5 | | | | |
| | SupplyIoOk | Bit 6 | | | | |
| | SupplyBusOk | Bit 7 | | | | |
| 162 | DigitalStatus | UINT | • | | | |
| | DigitalOutput3Overload | Bit 2 | | | | |
| | DigitalOutput4Overload | Bit 3 | | | | |
| **Direct I/O configuration** | | | | | | |
| 556 | CfO_DigitalDirection | UDINT | | | | • |
| 548 | CfO_DigitalFilter | UDINT | | | | • |
| 564<br>588 | CfO_AnalogFilter01<br>CfO_AnalogFilter02 | UDINT | | | | • |
| 572<br>596 | CfO_LowerLimit01<br>CfO_LowerLimit02 | UDINT | | | | • |
| 580<br>604 | CfO_UpperLimit01<br>CfO_UpperLimit02 | UDINT | | | | • |
| **Direct I/O communication** | | | | | | |
| 22 | AnalogOutput01 | INT | | | • | |
| 14<br>18 | AnalogInput01<br>AnalogInput02 | INT | • | | | |
| 9<br>11 | StatusInput01<br>StatusInput02 | USINT | • | | | |
| 5 | Digital outputs | USINT | | | • | |
| | DigitalOutput03 | Bit 2 | | | | |
| | ... | ... | | | | |
| | DigitalOutput07 | Bit 6 | | | | |
| 1 | Digital inputs I/II | USINT | • | | | |
| | DigitalInput01 | Bit 0 | | | | |
| | ... | ... | | | | |
| | DigitalInput08 | Bit 7 | | | | |
| 3 | Digital inputs II/II | USINT | • | | | |
| | DigitalInput09 | Bit 0 | | | | |

## 14.3 Module - Configuration

This module is equipped with 2 analog inputs. They can be connected individually or together via the same connection on the module.

### 14.3.1 Selecting the slots for the analog inputs

Name:
CfO_LedEnable_AI

The LedEnable register makes it possible to manually switch the LEDs on/off using connections 2 and 3.

| Data type | Value |
|---|---|
| USINT | See bit structure |

Bit structure:

| Bit | Name | Value | Information |
|---|---|---|---|
| 0 | Connection 2 - LED 1 | 0 | LED inactive |
| | | 1 | LED active |
| 1 - 2 | Reserved | - | |
| 3 | Connection 2 - LED 2 | 0 | LED inactive |
| | | 1 | LED active |
| 4 | Connection 3 - LED 1 | 0 | LED inactive |
| | | 1 | LED active |
| 5 - 6 | Reserved | - | |
| 7 | Connection 3 - LED 2 | 0 | LED inactive |
| | | 1 | LED active |

## 14.4 Module communication

### 14.4.1 Module status messages

Name:
ModuleStatus

This register is used to transfer general status messages for the module.

| Data type | Values |
|---|---|
| UINT | See the bit structure. |

Bit structure:

| Bit | Name | Value | Information |
|---|---|---|---|
| 0 - 1 | Reserved | - | |
| 2 | SensorSupplyX5Ok | 0 | Encoder power supply failure |
| | | 1 | Encoder power supply on connection 5 OK |
| 3 | SensorSupplyX1Ok | 0 | Encoder power supply failure |
| | | 1 | Encoder power supply on connection 1 OK |
| 4 | SensorSupplyX23Ok | 0 | Encoder power supply failure |
| | | 1 | Encoder power supply on connections 2 and 3 OK |
| 5 | SensorSupplyX48Ok | 0 | Encoder power supply failure |
| | | 1 | Encoder power supply on connections 4 and 8 OK |
| 6 | SupplyIoOk | 0 | I/O power supply outside the valid range |
| | | 1 | I/O power supply is OK |
| 7 | SupplyBusOk | 0 | Bus supply is outside the valid range |
| | | 1 | Bus supply is OK |

### 14.4.2 Status messages for the digital channels

Name:
DigitalStatus

This register is used to transfer general status messages for the digital channels.

| Data type | Values |
|---|---|
| UINT | See the bit structure. |

Bit structure:

| Bit | Name | Value | Information |
|---|---|---|---|
| 0 - 1 | Reserved | - | |
| 2 | DigitalOutput3Overload | 0 | Channel OK |
| | | 1 | Channel overloaded |
| 3 | DigitalOutput4Overload | 0 | Channel OK |
| | | 1 | Channel overloaded |
| 4 - 7 | Reserved | - | |

## 14.5 reACTION - Configuration

### 14.5.1 reACTION cycle time

Name:
ReActionCycleTimeValue
ReActionCycleTimeMultiplier

Registers "TimeValue" and "Multiplier" predefine the desired cycle time for the reACTION program. Register "TimeValue" contains the value, while register "Multiplier" contains the associated units.
Register "Multiplier" is currently permanently set to 1000 in order to predefine the cycle time with µs precision.

| Data type | Value |
|---|---|
| UDINT | 1 to 1310 |

### 14.5.2 Configuring the PAR data points

Name:
CfO_PARType01
CfO_PARType[02…04]

PAR data points can be defined for the reACTION program. To enable them, the desired data type must be made known according to the configuration in Automation Studio.

| Data type | Value |
|---|---|
| UDINT | See bit structure |

Bit structure:

| Bit | Name | Value | Information |
|---|---|---|---|
| 0 - 3 | Type01 - PAR 1<br>Type02 - PAR 9<br>Type03 - PAR 17<br>Type04 - PAR 25 | 0000 | Inactive |
| | | 0001 | USINT, BOOL |
| 4 - 7 | Type01 - PAR 2<br>Type02 - PAR 10<br>Type03 - PAR 18<br>Type04 - PAR 26 | 0010 | UINT |
| | | 0011 | UDINT |
| 8 - 11 | Type01 - PAR 3<br>Type02 - PAR 11<br>Type03 - PAR 19<br>Type04 - PAR 27 | 0100 | Reserved |
| | | 0101 | SINT |
| 12 - 15 | Type01 - PAR 4<br>Type02 - PAR 12<br>Type03 - PAR 20<br>Type04 - PAR 28 | 0110 | INT |
| | | 0111 | DINT |
| 16 - 19 | Type01 - PAR 5<br>Type02 - PAR 13<br>Type03 - PAR 21<br>Type04 - PAR 29 | 1000<br>…<br>1111 | Reserved |
| 20 - 23 | Type01 - PAR 6<br>Type02 - PAR 14<br>Type03 - PAR 22<br>Type04 - PAR 30 | | |
| 24 - 27 | Type01 - PAR 7<br>Type02 - PAR 15<br>Type03 - PAR 23<br>Type04 - PAR 31 | | |
| 28 - 31 | Type01 - PAR 8<br>Type02 - PAR 16<br>Type03 - PAR 24<br>Type04 - PAR 32 | | |

## 14.6 reACTION - Communication

At runtime, the reACTION module program is controlled via the program sequence in the CPU. In its active state, the reACTION program is then executed independently of the program sequence in the CPU.

### 14.6.1 Controlling the reACTION module

Name:
RTEnable
RTHardwareWarningQuit

This register controls the reACTION program.

| Data type | Value |
|---|---|
| USINT | See the bit structure. |

Bit structure:

| Bit | Name | Value | Information |
|---|---|---|---|
| 0 | RTEnable | 0 | Stops the reACTION program |
| | | 1 | Starts the reACTION program |
| 1 | Reserved | - | |
| 2 | RTHardwareWarningQuit | 0 | No effect |
| | | 1 | Acknowledges warning messages for the inputs and outputs |
| 3 - 7 | Reserved | - | |

### 14.6.2 reACTION module status messages

Name:
RTEngineRun
RTCycleTimeOverrun
RTHardwareWarning
RTFileInvalid
RTFunctionInvalid
RTInstanceInvalid
RTFileNotLoaded

This register is used to output various status messages.

| Data type | Value |
|---|---|
| USINT | See the bit structure. |

Bit structure:

| Bit | Name | Value | Information |
|---|---|---|---|
| 0 | RTEngineRun | 0 | reACTION program inactive |
| | | 1 | reACTION program active |
| 1 | RTCycleTimeOverrun | 0 | Configured RT cycle time observed |
| | | 1 | RT cycle time set too short |
| 2 | RTHardwareWarning<br>(group bit for acyclic status data points) | 0 | No status messages |
| | | 1 | Warning message for the inputs and outputs |
| 3 | Reserved | - | |
| 4 | RTFileInvalid<br>(invalid RT program preloaded) | 0 | RT program in RAM OK |
| | | 1 | RT program in RAM invalid[1)] |
| 5 | RTFunctionInvalid<br>(invalid software function) | 0 | RT program OK |
| | | 1 | RT program requesting invalid function block |
| 6 | RTInstanceInvalid<br>(invalid hardware instance) | 0 | RT program OK |
| | | 1 | RT program requesting invalid I/O |
| 7 | RTFileNotLoaded | 0 | Valid RT program in RT engine |
| | | 1 | No RT program loaded[2)] |

1) RTEnable has been enabled.

- A new or modified reACTION program has been detected but not yet verified as valid (duration depends on the size of the program).
- A new or modified reACTION program has been detected, but verification has failed.

2) RTEnable has been enabled but a valid reACTION program is not present in flash memory nor has it been temporarily downloaded to RAM.

### 14.6.3 Cycle counter for the active reACTION program

Name:
RTCycleCounter

Register "CycleCounter" can be used to determine how often the reACTION program has cycled.

| Data type | Value |
|---|---|
| UINT | 0 to 65535 |

### 14.6.4 Minimum cycle time of the active reACTION program

Name:
RTCycleTime

Register "RTCycleTime" can be used to determine how much time the reACTION module needs to cycle through the loaded program once.

| Data type | Value |
|---|---|
| UINT | 0 to 65535: Units 10 ns |

## 14.7 reACTION - Interaction

After startup, the reACTION program in the module runs independently. It reads the images of the required inputs and manages its assigned outputs throughout the entire network. In addition, the reACTION program can interact with the CPU. There are 3 different data point types available for this.

### 14.7.1 PAR data points

Name:
PAR[01...32]
PAR[01...32]_Bit1
PAR[01...32]_Bit2
PAR[01...32]_Bit3
PAR[01...32]_Bit4
PAR[01...32]_Bit5
PAR[01...32]_Bit6
PAR[01...32]_Bit7
PAR[01...32]_Bit8

Once enabled, the PAR data points are transported cyclically via X2X Link. They are used to transfer information from the CPU to the reACTION program. They can be used to intervene in the execution of the reACTION program.

## Information:

**PAR data points DO NOT control the module's outputs directly!**

| Data type | Value |
|---|---|
| (U)SINT, BOOL | Corresponding range of values |
| (U)INT | |
| (U)DINT | |

| Register | Name | Data type | Read | | Write | |
|---|---|---|---|---|---|---|
| | | | Cyclic | Acyclic | Cyclic | Acyclic |
| 4095 + Index * 8 | PAR01<br>PAR[02...32] | (U)SINT | | | • | |
| | PAR01_Bit1<br>PAR[02...32]_Bit1 | Bit 0 | | | | |
| | PAR01_Bit2<br>PAR[02...32]_Bit2 | Bit 1 | | | | |
| | PAR01_Bit3<br>PAR[02...32]_Bit3 | Bit 2 | | | | |
| | PAR01_Bit4<br>PAR[02...32]_Bit4 | Bit 3 | | | | |
| | PAR01_Bit5<br>PAR[02...32]_Bit5 | Bit 4 | | | | |
| | PAR01_Bit6<br>PAR[02...32]_Bit6 | Bit 5 | | | | |
| | PAR01_Bit7<br>PAR[02...32]_Bit7 | Bit 6 | | | | |
| | PAR01_Bit8<br>PAR[02...32]_Bit8 | Bit 7 | | | | |
| 4094 + Index * 8 | PAR01<br>PAR[02...32] | (U)INT | | | • | |
| 4092 + Index * 8 | PAR01<br>PAR[02...32] | (U)DINT | | | • | |

### 14.7.2 RES data points

Name:
RES[01...32]
RES[01...32]_Bit1
RES[01...32]_Bit2
RES[01...32]_Bit3
RES[01…32]_Bit4
RES[01...32]_Bit5
RES[01...32]_Bit6
RES[01...32]_Bit7
RES[01...32]_Bit8

Once enabled, the RES data points are transported cyclically via X2X Link. They are used to transfer information from the reACTION program to the CPU.

## Information:

**RES data points DO NOT map the module's input directly!**

| Data type | Value |
|---|---|
| (U)SINT, BOOL | Corresponding range of values |
| (U)INT | |
| (U)DINT | |

| Register | Name | Data type | Read | | Write | |
|---|---|---|---|---|---|---|
| | | | Cyclic | Acyclic | Cyclic | Acyclic |
| 5119 + Index * 8 | RES01<br>RES[02…32] | (U)SINT | • | | | |
| | RES01_Bit1<br>RES[02…32]_Bit1 | Bit 0 | | | | |
| | RES01_Bit2<br>RES[02…32]_Bit2 | Bit 1 | | | | |
| | RES01_Bit3<br>RES[02…32]_Bit3 | Bit 2 | | | | |
| | RES01_Bit4<br>RES[02…32]_Bit4 | Bit 3 | | | | |
| | RES01_Bit5<br>RES[02…32]_Bit5 | Bit 4 | | | | |
| | RES01_Bit6<br>RES[02…32]_Bit6 | Bit 5 | | | | |
| | RES01_Bit7<br>RES[02…32]_Bit7 | Bit 6 | | | | |
| | RES01_Bit8<br>RES[02…32]_Bit8 | Bit 7 | | | | |
| 5118 + Index * 8 | RES01<br>RES[02…32] | (U)INT | • | | | |
| 5116 + Index * 8 | RES01<br>RES[02…32] | (U)DINT | • | | | |

### 14.7.3 PVAR and RVAR data points

Name:
PVAR[1...256]
RVAR[1...256]

In addition to PAR and RES data points, VAR data points can also be defined in the reACTION program. They are a direct component of the reACTION program and can be accessed acyclically by the CPU. Like the PAR and RES data points, the PVAR data points are used to transfer information from the CPU to the reACTION program. The RVAR data points are used to transfer feedback from the reACTION program to the CPU.

| Data type | Value |
|---|---|
| DINT | -2,147,483,648 to 2,147,483,647 |

| Register | Name | Data type | Read | | Write | |
|---|---|---|---|---|---|---|
| | | | Cyclic | Acyclic | Cyclic | Acyclic |
| 6140 + Index * 8 | PVAR1<br>PVAR[2...256] | DINT | | | | • |
| 6140 + Index * 8 | RVAR1<br>RVAR[2...256] | DINT | | • | | |

## 14.8 reACTION function blocks - General

The following tables provide an overview of I/O channel assignments to reACTION function blocks.

### Digital inputs/outputs

| Channel | Function block | | |
|---|---|---|---|
| | Mapping[1)] | rtiDin | rtiDout, rtiDoutTime |
| X1: DI 1 | 0x00 | Channel 1 | |
| X1: DI 2 | 0x01 | Channel 2 | |
| X5: DI 3 / DO 3 | 0x02 | Channel 3 | Channel 3 |
| X5: DI 4 / DO 4 | 0x03 | Channel 4 | Channel 4 |
| X8: DI 5 / DO 5 | 0x04 | Channel 5 | Channel 5 |
| X8: DI 6 / DO 6 | 0x05 | Channel 6 | Channel 6 |
| X8: DI 7 / DO 7 | 0x06 | Channel 7 | Channel 7 |
| X8: DI 8 | 0x07 | Channel 8 | |
| X8: DI 9 | 0x08 | Channel 9 | |

1) The "Mapping" specification is needed in the event that multiple physical inputs/outputs must be grouped together in order to be processed by a reACTION function block (e.g. rtiABRPos) (see "reACTION function blocks - Configuration" on page 30).

### Analog inputs

| Channel | Function block | | |
|---|---|---|---|
| | Mapping[1)] | rtiAin | rtiAout |
| X2/X3: AI 1 | 0x00 | Channel 1 | |
| X2/X3: AI 2 | 0x01 | Channel 2 | |

1) The "Mapping" specification is needed in the event that multiple physical inputs/outputs must be grouped together in order to be processed by a reACTION function block (e.g. rtiABRPos) (see "reACTION function blocks - Configuration" on page 30).

### Analog output

| Channel | Function block | | |
|---|---|---|---|
| | Mapping[1)] | rtiAin | rtiAout |
| X4: AO 1 | 0x00 | | Channel 1 |

1) The "Mapping" specification is needed in the event that multiple physical inputs/outputs must be grouped together in order to be processed by a reACTION function block (e.g. rtiABRPos) (see "reACTION function blocks - Configuration" on page 30).

## 14.9 reACTION function blocks - Configuration

Some function blocks in library AsIoRti must be configured before they can be used.

| Function block | Information |
|---|---|
| rtiABRPos | The module offers the option of using function block rtiABRPos once in the reACTION program. To do so, the function block must be assigned 3 digital inputs that are no longer available for rtiDin. |
| rtiABCnt | The module offers the option of using function block rtiABCnt up to 3 times in the reACTION program. To do so, the function blocks must be assigned 2 digital inputs as an A or B track that are no longer available for rtiDin.<br>In addition, an external event can be defined for each rtiABCnt function block. The input used for this is also no longer available for rtiDin. |

Table 5: List of function blocks requiring prior configuration

### 14.9.1 Function blocks rtiABRPos and rtiABCnt

Function blocks rtiABRPos and rtiABCnt can be used to process the position value of an ABR incremental encoder in a reACTION task. Several hardware channels of the module are used for this. The incoming signals are interpreted by the reACTION engine and converted into a location.

The update rate depends on both the reACTION engine and the hardware used. The reACTION engine is basically able to calculate positions with an update rate of up to 8 MHz. The input frequencies of the hardware inputs can be taken from the technical data of the respective module.

These function blocks can be used separately or in combination.

#### Using function block rtiABRPos

The following points must be taken into account when using function block rtiABRPos in a reACTION program:

- The function block can only be used once in a reACTION program.
- 3 digital inputs must be defined on the module for input signals A, B and R.
- In addition, 1 digital input of the module can be defined as an event input.

Example diagram of input signals:

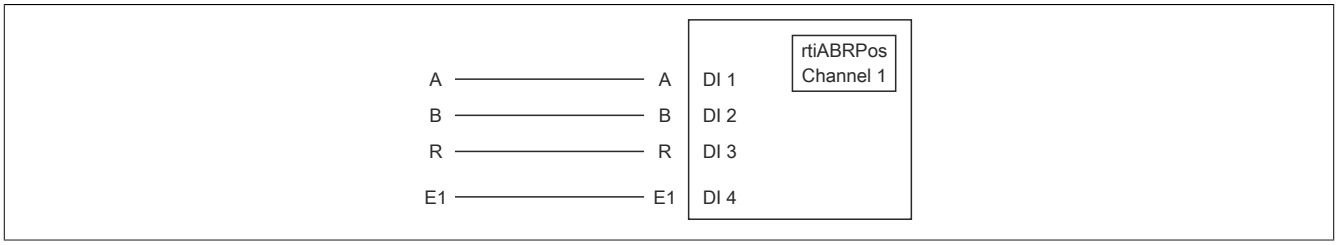



Figure 1: Schematic diagram of input signals for rtiABRPos

### Using function block rtiABCnt

The following points must be taken into account when using function block rtiABCnt in a reACTION program:

- The function block can be used up to 3 times in a reACTION program.
- 2 digital inputs must be defined on the module for input signals A and B.
- In addition, up to 3 digital inputs on the module can be defined as event inputs E1, E2 and E3.

Example diagram of input signals:

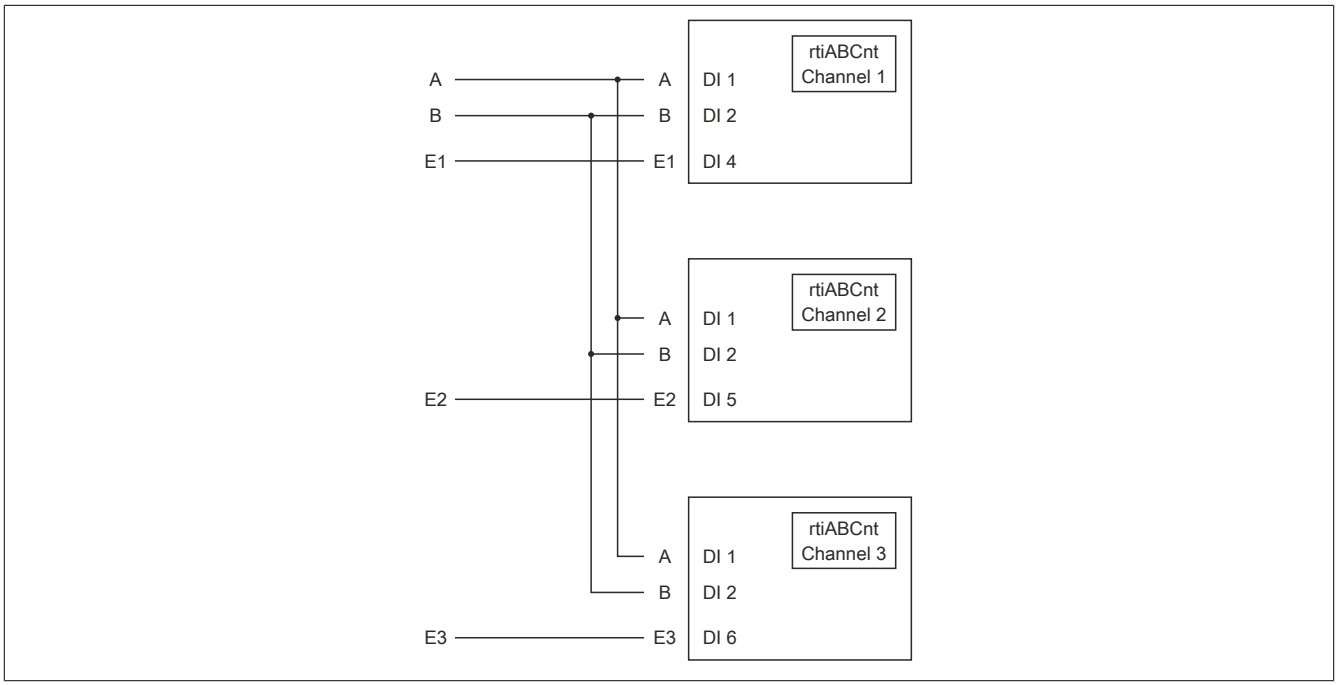



Figure 2: Schematic diagram of input signals for rtiABCnt

### Using function blocks rtiABRPos and rtiABCnt in combination

The following points must be taken into account when using function blocks rtiABRPos and rtiABCnt together in a reACTION program:

- Function block rtiABRPos can only be used once in a reACTION program.
- Function block rtiABCnt can be used up to 2 times in a reACTION program.
- 3 digital inputs must be defined for input signals A, B and R (rtiABRPos).
- The same digital inputs are used for input signals A and B (rtiABCnt).
- In addition, up to 3 event inputs E1, E2 and E3 can be defined (rtiABCnt).
- E1 is used for the event input (rtiABRPos).

Example diagram of input signals:

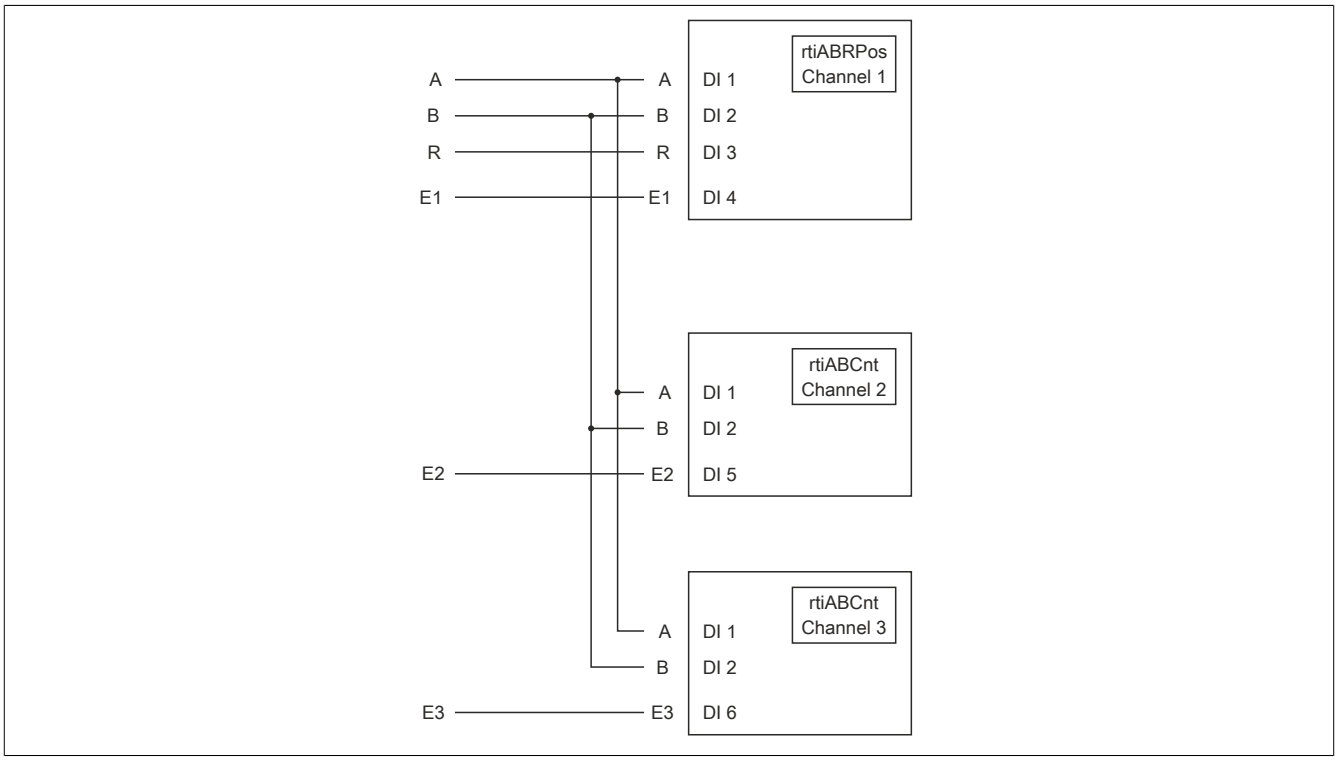



Figure 3: Diagram of input signals when using rtiABRPos and rtiABCnt at the same time

#### 14.9.1.1 Registering the position encoder (rtiABRPos/rtiABCnt)

Name:
CfO_Config_ABR1

This register specifies the technical characteristics of the connected ABR incremental encoder:

| Data type | Values |
|---|---|
| UDINT | See the bit structure. |

Bit structure:

| Bit | Description | Value | Information |
|---|---|---|---|
| 0 - 15 | Increments per revolution | 0 to 65535 | Reference pulse monitoring:<br>If the reference pulse is different than defined here, this is indicated on the status output of function block rtiABRPos. |
| 16 | Inversion of the counting direction set by signals A and B | 0 | Positive counting direction |
| | | 1 | Negative counting direction |
| 17 - 31 | Reserved | 0 | |

#### 14.9.1.2 Wiring the position encoder (rtiABRPos/rtiABCnt)

Name:
CfO_ChannelMapping1_ABR1
CfO_ChannelMapping2_ABR1

Before function blocks rtiABRPos/rtiABCnt can be processed by the reACTION engine, the hardware inputs to be used by the ABR incremental encoder must be defined on the module. The "ChannelMapping" registers define which input is interpreted as the A, B, R, E1, E2 and E3 signal.

| Data type | Values |
|---|---|
| UDINT | See the bit structure. |

Bit structure of CfO_ChannelMapping1_ABR1:

| Bit | Description | Value | Information |
|---|---|---|---|
| 0 - 7 | Input E1 | 0 | Mapped to digital input 1 |
| | | 1 | Mapped to digital input 2 |
| | | ... | ... |
| | | 7 | Mapped to digital input 8 |
| | | 8 to 255 | Reserved |
| 8 - 15 | Input R | 0 to 255 | For possible values, see bits 0 to 7. |
| 16 - 23 | Input B | 0 to 255 | For possible values, see bits 0 to 7. |
| 24 - 31 | Input A | 0 to 255 | For possible values, see bits 0 to 7. |

Bit structure of CfO_ChannelMapping2_ABR1:

| Bit | Description | Value | Information |
|---|---|---|---|
| 0 - 15 | Reserved | 0 | |
| 16 - 23 | Input E3 | 0 | Mapped to digital input 1 |
| | | 1 | Mapped to digital input 2 |
| | | ... | ... |
| | | 7 | Mapped to digital input 8 |
| | | 8 to 255 | Reserved |
| 24 - 31 | Input E2 | 0 to 255 | For possible values, see bits 16 to 23. |

## Information:

**For information about the relationship between the input on the module and the channel name, see section "reACTION function blocks - General".**

#### 14.9.1.3 Position encoder scaling (rtiABRPos)

Name:
CfO_ScalingUnits_ABR1

CfO_ScalingIncrements_ABR1

An optional gear ratio can be configured using registers "Units" and "Increments". The dividend for scaling is defined in register "Units"; the divisor is defined in register "Increments".

| Data type | Values | Information |
|---|---|---|
| UDINT | 0 to 4,294,967,295 | CfO_ScalingUnits_ABR1: Units per interval<br>CfO_ScalingIncrements_ABR1: Increments per interval |

**Formula for calculation**

Scaling ratio = ScalingUnits / ScalingIncrements

**Example 1**

ScalingUnits = 1
ScalingIncrements = 1

Position value (Pos) = ABR increments * ScalingUnits / ScalingIncrements
Position value (Pos) = ABR increments * 1/1

In this example, the ABR position value is output unchanged on output "Pos".

**Example 2**

ScalingUnits = 10
ScalingIncrements = 4

Position value (Pos) = ABR increments * ScalingUnits / ScalingIncrements
Position value (Pos) = ABR increments * 10/4

In this example, the ABR position value is multiplied by 2.5 and output on output "Pos".

## Information:

**The encoder values are calculated internally as INT64 values in 32.32 format. On output "Pos" of function block "rtiABRPos", only the whole number value (INT32) is output for the user. The fixed point decimal places are used internally to calculate a higher resolution.**

## 14.10 Direct I/O configuration

This module is equipped with 3 analog and 9 digital channels. When using the "Direct I/O" function model, these channels can be adapted to the requirements of the specific application.

### 14.10.1 Direction of digital channels

Name:
CfO_DigitalDirection

This register determines the signal direction of digital channels 3 to 7.

| Data type | Values |
|---|---|
| UDINT | See the bit structure. |

Bit structure:

| Bit | Name | Value | Information |
|---|---|---|---|
| 0 - 1 | Reserved | 0 | |
| 2 | Direction - Digital channel 3 | 0 | Input |
| | | 1 | Output |
| ... | ... | ... | |
| 6 | Direction - Digital channel 7 | 0 | Input |
| | | 1 | Output |
| 7 | Reserved | 0 | |

### 14.10.2 Filtering digital channels

Name:
CfO_DigitalFilter

This register defines the filter time of the digital channels. The filter value affects both the switching delay as well as the immunity of the channels.

| Data type | Value |
|---|---|
| UDINT | 0 to 500000: Units 10 ns |

### 14.10.3 Filtering analog inputs

Name:
CfO_AnalogFilter01 to CfO_AnalogFilter02

This register is used to define the filter level of the associated analog channel. The filter value affects both the ADC conversion rate as well as the precision of the analog value being read.

| Data type | Value |
|---|---|
| UDINT | 0 to 15 |

### 14.10.4 Upper and lower limits of analog inputs

Name:
CfO_LowerLimit01, CfO_UpperLimit01
CfO_LowerLimit02, CfO_UpperLimit02

These register define the lower/upper limit value of the associated analog inputs. If the converted value violates the user-defined limits, then a corresponding status message is output.

| Data type | Value |
|---|---|
| UDINT | -32767 to 32767 |

## 14.11 Direct I/O communication

This module is equipped with the following inputs and outputs:

- 1 analog output of type ±10 V
- 2 analog inputs of type ±10 V,
- 4 digital inputs (sink) of type 24 VDC,
- 2 digital channels configurable as inputs (sink) or outputs (source) for 24 VDC
- 3 digital channels configurable as inputs (sink) or outputs (source) of type 5 V diff.

### 14.11.1 Analog output

Name:
AnalogOutput01

This register is used to predefine the value to be output by the analog output.

| Data type | Value |
|---|---|
| INT | -32767 to 32767 |

### 14.11.2 Analog inputs

Name:
AnalogInput01
AnalogInput02

This register is used to depict the value read from the respective analog input.

| Data type | Value |
|---|---|
| INT | -32767 to 32767 |

### 14.11.3 Status feedback from analog inputs

Name:
StatusInput01 to StatusInput02

This register is used to depict the status feedback from the respective analog input.

| Data type | Values |
|---|---|
| USINT | See the bit structure. |

Bit structure:

| Bit | Name | Value | Information |
|---|---|---|---|
| 0 | Broken wire | 0 | No error |
| | | 1 | Open circuit |
| 1 | Overflow | 0 | No error |
| | | 1 | Violation - Upper limit value |
| 2 | Underrun | 0 | No error |
| | | 1 | Violation - Lower limit value |
| 3 - 7 | Reserved | 0 | |

### 14.11.4 Digital outputs

Name:
DigitalOutput03 to DigitalOutput07

This register is used to predefine the value that should be signaled on the digital output.

| Data type | Values |
|---|---|
| USINT | See the bit structure. |

Bit structure:

| Bit | Name | Value | Information |
|---|---|---|---|
| 0 - 1 | Reserved | 0 | |
| 2 | DigitalOutput03 | 0 | FALSE |
| | | 1 | TRUE |
| ... | ... | ... | |
| 6 | DigitalOutput07 | 0 | FALSE |
| | | 1 | TRUE |
| 7 | Reserved | 0 | |

### 14.11.5 Digital inputs

Bit structure 1 name:
DigitalInput01 to DigitalInput08

Bit structure 2 name:
DigitalInput09

This register is used to depict the value read from the respective digital input.

| Data type | Value |
|---|---|
| USINT | See bit structures. |

Bit structure 1:

| Bit | Name | Value | Information |
|---|---|---|---|
| 0 | DigitalInput01 | 0 | FALSE |
| | | 1 | TRUE |
| ... | ... | ... | |
| 7 | DigitalInput08 | 0 | FALSE |
| | | 1 | TRUE |

Bit structure 2:

| Bit | Name | Value | Information |
|---|---|---|---|
| 0 | DigitalInput09 | 0 | FALSE |
| | | 1 | TRUE |

## 14.12 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

| Minimum cycle time |
|---|
| ≥200 µs |

## 14.13 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

| Minimum I/O update time |
|---|
| ≥200 µs |